

In re Patent Application of:

AMMAR

Serial No. 09/862,982

Filing Date: May 22, 2001

REMARKS

Claims 1-15 remain in this application. Claims 16-20 have been canceled. Claims 1 and 10 have been amended.

Applicant thanks the Examiner for the detailed study of the application and prior art.

At the outset, Applicant stresses that the present claimed invention is more than a package for an integrated circuit with a coefficient of thermal expansion matched base plate and integrated circuit as appears to be the conclusion reached by the Examiner.

The present claimed invention is a microwave monolithic integrated circuit (MMIC) package that uses a single MMIC and base plate that is matched to its coefficient of thermal expansion (CTE) with the single MMIC. The solder preform is contained on the base plate. The MMIC is mounted on the solder preform and secured together by a solder flow process. A chip cover covers the MMIC. The base plate and chip cover are configured with respective portions that engage each other such that any pads on the MMIC are exposed for wire and ribbon bonding thereto.

This claimed structure is clearly shown in the drawings (FIGS. 2A and 2B) where open areas are formed at the top and side of corners to leave exposed any pads 50 on the MMIC for wire and ribbon bonding. The cover is shaped such that it does not cover chip input and output pads and DC pads, such as a gate and drain. Respective portions of the base plate and chip cover engage each to form the package that protects the MMIC, but allows the functionality as described.

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The present claimed invention is a MMIC package having low cost and low signal losses, compared to prior art IC packages. Prior art packages typically use an intermediate connection method between the chip and other external circuits, such as leads or ball grid arrays or waveguide transitions as described in the cited prior art. Because of its simplicity, the present claimed invention can be formed in a one step fabrication requiring only an automated pick and place machine instead of a multi-step assembly process. The present invention can protect very fragile (such as 2 to about 4 mil thick) gallium arsenide MMIC chips.

The Examiner has rejected all claims as obvious over U.S. Patent No. 6,064,286 to Ziegner et al. (hereinafter "Ziegner") in view of U.S. Patent No. 5,932,927 to Koizumi et al. (hereinafter "Koizumi") and U.S. Patent No. 5,528,074 to Goto et al. (hereinafter "Goto") (Claims 1-3 and 6-15) and other dependent claims as obvious over those references in view of U.S. Patent No. 5,596,171 to Harris et al. (hereinafter "Harris") in view of U.S. Patent No. 4,359,754 to Hayakawa et al. (hereinafter "Hayakawa").

Applicant agrees that Ziegner discloses a CTE matched material base plate and cover and a package that can be mounted on a printed wiring board (PWB) or directly on a support plate. It is clear that Ziegner describes a millimeter wave package for a multi-chip circuit using a dielectric substrate, metallization circuitry and some semiconductor components with a waveguide transition. The present claimed invention is directed to a single MMIC chip

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package and no restriction with the type of DC or RF interfaces.

The Ziegner package uses intermediate interconnects that can wrap around the package (column 8, line 37) while the present claimed invention requires no intermediate interconnects and thereby adds no losses.

It is also clear that Ziegner uses an integrated circuit 30 having a number of semiconductor die and interconnects, including a dielectric resonator DR puck that is positioned on the glass substrate. These many components and die form a large circuit with multiple chips and nowhere suggests a single MMIC chip package as in the present claimed invention. Ziegner requires a structure having intermediate interconnects as compared to the present claimed invention where no intermediate interconnects are required. The structure in Ziegner also uses chimney structures for waveguides and a two-part base. This is clearly set forth in column 6, starting at lines 1-28, and column 7, starting at line 27-58 as set forth below:

"First, the interconnects 26 are installed on the base 22. This can be performed using a hot-bar B-stage epoxy attachment process as one having ordinary skill in the art would recognize. Then, a dark color epoxy ink is deposited in fiducial recesses 79 in the base 22 for optical alignment contrast in assembly. Next, a low modulus conductive epoxy is applied to the top surface 42 of the base 22 using a screen printing process or a pad printing process as one having ordinary skill in

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the art would recognize. Preferably, the epoxy is applied in a preferred pattern in the area where the integrated circuit 30 is to be attached on the base 22. Then, the integrated circuit 30 is positioned on the top surface 42 of the base 22, and the low modulus conductive epoxy is cured. Then, the semiconductor die are attached to the integrated circuit 30 and the interconnects 26 are connected to the integrated circuit 30 using a thermosonic wire bonding or flip chip attachment process. Next, if a dielectric resonator 64, such as a DR puck, is to be provided on the integrated circuit 30, epoxy is deposited on the integrated circuit 30 in the position in which the dielectric resonator 64 is desired. Then, the dielectric resonator 64 is placed on the epoxy, and the epoxy is cured. Next, an epoxy seal ring is applied to a seal edge of the cover 24, the cover 24 is attached to the base 22, and the epoxy seal ring is cured. Subsequently, the package 20 is preferably subjected to electrical testing before the package 20 is mounted on a printed wiring board 36 or other substrate as shown in FIG. 3."

* * * *

"The package 20a illustrated in FIG. 9 will now be described, and FIGS. 9-13, as well as FIG. 8, relate thereto. As shown in FIG. 9, package 20a, like package 20, also includes a base 22a and a cover 24a adhered to the base 22a to form a housing.

As shown in FIG. 12, the bottom surface 46a of the base 22a includes a chimney structure 48a which has three waveguide ports 44a formed therein for receiving waveguides of an integrated circuit 30a.

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As shown in FIG. 11, the integrated circuit 30a is mounted on a top surface 42a of the base 22a, and preferably includes a dielectric resonator 64a such as a DR puck which is shielded by a region 68a defined by a wall 66a of the cover 24a when the cover 24a is contacted with the base 22a. As with the package 20 shown in FIG. 1, preferably the integrated circuit 30a mounted in package 20a on the base 22a thereof is a millimeter wave circuit 32a mounted on a glass substrate 34a.

Essentially, the main difference between the package 20a depicted in FIG. 9 and the package 20 depicted in FIG. 1, and already described, is that interconnects 26a of the package 20a illustrated in FIG. 9 wrap around the edges of the base 22a to the bottom surface 46a of the base 22a rather than outwardly extend from a perimeter of the base 22a. This can best be viewed in FIG. 11. As a result, the spring clip 28a which is used to mount the package 20a, does not include outwardly extending portions for contactably pressing the interconnects 26a into contact with conductive traces 38 when the package is mounted. Similar to the package 20 shown in FIG. 1, the package 20a preferably provides, as shown in FIG. 10, that the chimney structure 48a on the base 22a of the package 20a extends to the other side of a support plate 40."

As to Koizumi, the Examiner uses this reference to suggest a high frequency device comprising a microwave integrated circuit 1 mounted on a base 2 by way of solder. Applicant notes that the Koizumi package is a typical prior

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art package for high frequency device packaging using electrodes for ground and signal, and multiple leads for electrical connections, a tape carrier, and a resin body. Again, as noted before, the present claimed invention is a simple construction at low cost and does not require the use of leads or intermediate connects.

Applicant notes that the Examiner agrees that Ziegner and Koizumi do not disclose or suggest a MMIC package where pads on the MMIC are exposed to wire and ribbon bonding. Thus, the Examiner must combine a third reference, Goto (FIG. 9), to bolster the argument of unpatentability. The Examiner argues that Goto discloses a microwave semiconductor device as a gallium arsenide substrate (chip) and lid (cover) 40f that has holes 48 which expose the gallium arsenide substrate and permit waveguides 12a, 12h to connect to the substrate.

Applicant notes that Goto in FIG. 9 shows a possible RF connection through a hole in the cover, which reduces losses, but fails to describe how the MMIC chip DC and ground connections can be achieved. The present claimed invention has a packaging that provides a direct path for all DC, ground and RF connections with no limitations or restrictions. The user may use wire bonds, ribbon bonds, direct leads or leadless waveguide transitions with the present claimed invention.

It is clear that Ziegner, Koizumi and Goto nowhere disclose or suggest Applicant's claimed invention using the

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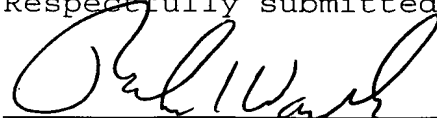
single MMIC, base plate, solder preform and chip cover as described and claimed.

As to the other cited prior art reference, Harris discloses a prior art semiconductor die package, such as for field effect transistors, and not MMICs. The package conductor rests against a circuit board and semiconductor device with a package lid or cover 104. The use of the plastic cover in Harris is much different and nowhere suggests the novel and unobvious structure of the present claimed invention.

As to Hayakawa, it is directed to a semiconductor device for amplifying microwave signals. It uses field effect transistor chips that are soldered. Nowhere does it suggest the present claimed invention as set forth in the present Amendment.

Applicant contends that the present case is in condition for allowance and respectfully requests that the Examiner issue a Notice of Allowance and Issue Fee Due. If the Examiner has any questions or suggestions for placing this case in condition for allowance, the undersigned attorney would appreciate a telephone call.

Respectfully submitted,



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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: **DIRECTOR, U.S. PATENT AND TRADEMARK OFFICE, WASHINGTON, DC 20231**, on this 18th day of February, 2003.

Julie Lalan